This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (currently amended): An apparatus for performing low density parity check encoding operations, the apparatus comprising:

memory including a set of memory locations for storing L ~~sets of~~ Z-bit vectors, where Z is a positive integer greater than one and L is a positive integer;

a vector unit operation processor including a circuit for performing Z parity calculations in parallel to compute a Z-bit vector, each bit of the computed Z-bit vector being generated by one of the Z parity calculations, an accumulator for storing the computed Z-bit vector, and an output device for passing the computed Z-bit vector to ~~the~~ said memory ~~in response to operation instructions~~; and

a ~~switching~~ reordering device coupled to the memory and to the vector unit operation processor, the ~~switching~~ reordering device for passing ~~a~~ Z-bit vectors ~~vector~~ between said memory and said vector unit operation processor and for performing a bit level reordering operation on elements of at least one Z-bit vector, in response to ~~switch~~ reordering control information, as the at least one Z-bit vector is passed between said memory and said vector unit operation processor by said reordering device.

Claim 2 (original): The apparatus of claim 1, further comprising:

an ordering control module coupled to said memory for generating read and write indices; and

an operation control module coupled to said vector unit operation processor for generating unit operation instructions.

Claim 3 (currently amended): The apparatus of claim 2, wherein the ordering control module is further coupled to said reordering ~~switch~~ device for generating said reordering ~~switch~~

control information used to control the ~~switching of~~ reordering for said at least one Z-bit vector.

Claim 4 (currently amended): The apparatus of claim 1, wherein the ~~switching~~ reordering device includes circuitry for performing a vector ~~rotation~~ element reordering operation that includes a bitwise rotation operation to generate a reordered ~~rotated~~ Z-bit vector.

Claim 5 (currently amended): The apparatus of claim 2, wherein the ordering control module stores information on the order ~~of~~ the Z-bit vectors are to be read out of the memory and information on the order ~~of~~ the Z-bit vectors are to be written into the memory.

Claim 6 (currently amended): The apparatus of claim 5 ~~2~~, wherein the ordering control module further stores bitwise rotation operation information ~~on the rotation~~ to be used in generating said re-ordering control information ~~performed on the read-out vectors from said memory by said switch~~.

Claim 7 (original): The apparatus of claim 2, wherein the ordering control module sequentially generates index identifiers, each identifier controlling the memory to access memory locations corresponding to a vector as part of a single SIMD instruction.

Claim 8 (original): The apparatus of claim 7, wherein each identifier is a single memory address.

Claim 9 (original): The apparatus of claim 2, wherein said operation control module stores operation instructions, each instruction controlling the operation at said vector unit operation processor.

Claim 10 (original): The apparatus of claim 9, wherein the operation control module sequentially generates operation

instructions, each instruction controlling said vector unit operation processor to perform instructed operations.

Claim 11 (currently amended): The apparatus of claim 4 ~~2~~, further comprising an encoder control module coupled to said ordering control module, the encoder control module including means for supplying information to said ordering control module used to control the order in which each of the L Z-bit vectors is to be read out of said memory, their associated reorderings ~~rotations~~, and the order to be written into said memory.

Claim 12 (currently amended): The apparatus of claim 11, wherein the encoder control module ~~device~~ is further coupled to said operation control module, the encoder control device including means for supplying information to said operation control module used to generate operation instructions.

Claim 13 (currently amended): A method of performing low density parity check encoding operations, the method comprising:

storing L ~~sets of~~ Z-bit vectors in a memory device, where Z is a positive integer greater than one and L is a positive integer;

reading one of said ~~sets of Z bit~~ L stored Z-bit vectors from said memory device ~~stored L sets of Z bit vectors~~;

~~rotating~~ performing a bit level reordering of the bits in said read one of said ~~Z bit~~ Z-bit vectors; and

operating a vector unit processor to perform a plurality of parity check combining operations in parallel to combine the bits of the ~~rotated~~ reordered ~~Z bit~~ Z-bit vector with a Z-bit vector stored in said vector unit processor to generate a new Z-bit vector.

Claim 14 (currently amended): The method of claim 13, further comprising:

storing said new ~~z-bit~~ Z-bit vector in said memory device in the place of one of the L stored ~~L sets of Z bit~~ Z-bit vectors.

Claim 15 (currently amended): The method of claim 14, wherein said parity check combining operations performed by said vector unit processor are exclusive OR operations.

Claim 16 (currently amended): ~~The method of claim 15~~ A method of performing encoding operations, the method comprising:

storing L Z-bit vectors in a memory device, where Z is a positive integer greater than one and L is a positive integer;

reading one of said L stored Z-bit vectors from said memory device;

reordering the bits in said read one of said Z-bit vectors; and

operating a vector unit processor to perform a plurality of combining operations to combine the bits of the reordered Z-bit vector with a Z-bit vector stored in said vector unit processor to generate a new Z-bit vector

storing said new Z-bit vector in said memory device in the place of one of the L stored Z-bit vectors

wherein said combining operations performed by said vector unit processor are exclusive OR operations; and

wherein said encoding method is a low density parity check encoding method.

Claim 17 (currently amended): The method of claim 14, further comprising:

executing a set of stored machine executable instructions to control the ~~rotation~~ reordering of the read Z bit vector, said reordering including a rotation operation.

Claim 18 (currently amended): The method of claim 14, further comprising:

using the executed set of stored machine executable instructions to determine which one of said L ~~sets of~~ stored ~~z bit~~ Z-bit vectors is to be read from memory.

Claim 19 (currently amended): The method of claim 14, further comprising:

using the executed set of stored machine executable instructions to determine when one of said ~~sets of~~ L stored ~~z bit~~ Z-bit vectors is to be read from memory.

Claim 20 (currently amended): The method of claim 19, further comprising:

using the executed set of stored machine executable instructions to determine which one of the L stored ~~L sets of z bit~~ Z-bit vectors is to be replaced by storing the new ~~z bit~~ Z-bit vector in said memory device.

Claim 21 (currently amended): The method of claim 19, further comprising:

resetting the ~~z bit~~ Z-bit vector stored in said vector unit processor at the same time said new ~~z bit~~ Z-bit vector is stored.

Claim 22 (currently amended): The method of claim 14, further comprising:

resetting the ~~z bit~~ Z-bit vector stored in said vector unit processor at the same time said new ~~z bit~~ Z-bit vector is stored.

Claim 23 (currently amended): The method of claim 14, further comprising:

using the executed set of stored machine executable instructions to determine which one of the L stored ~~L sets of z bit~~ Z-bit vectors is to be replaced by storing the new ~~z bit~~ Z-bit vector in said memory device.

Claim 24 (currently amended): A method of performing low density parity check encoding operations, the method comprising:

storing L ~~sets of~~ Z-bit vectors in a memory device, where Z is a positive integer greater than one and L is a positive integer;

reading one of said ~~sets of~~ Z bit vectors from said stored L sets of ~~Z bit~~ Z-bit vectors;

operating a vector unit processor to perform a plurality of parity check combining operations in parallel to combine the bits of the ~~rotated Z bit~~ read Z-bit vector with a Z-bit vector stored in said vector unit processor to generate a new Z-bit vector;

~~rotating~~ reordering the bits in said new ~~Z bit~~ Z-bit vector by performing a bit level reordering of bits in the new Z-bit vector to produce a reordered Z-bit vector; and

storing said reordered ~~rotated new Z bit~~ Z-bit vector in said memory device in the place of one of the L stored ~~L sets of Z bit~~ Z-bit vectors.

Claim 25 (currently amended): ~~The method of claim 24,~~ A method of performing encoding operations, the method comprising:

storing L Z-bit vectors in a memory device, where Z is a positive integer greater than one and L is a positive integer;

reading one of said Z-bit vectors from said L stored Z-bit vectors;

operating a vector unit processor to perform a plurality of combining operations to combine the bits of the read Z-bit vector with a Z-bit vector stored in said vector unit processor to generate a new Z-bit vector;

reordering the bits in said new Z-bit vector by cyclicly shifting the position of bits in the new Z-bit vector to implement a cyclic shift operation that produces a reordered Z-bit vector; and

storing said reordered Z-bit vector in said memory device in the place of one of the L stored Z-bit vectors;

wherein said combining operations performed by said vector unit processor are exclusive OR operations; and

wherein said encoding method is a low density parity check encoding method.

Claim 26 (currently amended): The method of claim 25, further comprising:

executing a set of stored machine executable instructions to control the reordering ~~rotation~~ of the read ~~Z~~ ~~bit~~ Z-bit vector and to determine which one of the L stored ~~L~~ ~~sets of~~ ~~Z bit~~ Z-bit vectors is to be replaced by storing said ~~rotated new Z bit~~ reordered Z-bit vector in said memory device.